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| EXAMINER | |
|---|---|
| ELMORE, REBA I | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2187 | 11 |

DATE MAILED: 11/19/2001

Please find below and/or attached an Office communication concerning this application or proceeding.



MG

| Office Action Summary | Application No. 09/205,086 | Applicant(s) BOGIN ET AL. | |
|---|---|---|---|
| | Examiner REBA I. ELMORE | Art Unit 2187 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *31 July 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-28 and 38-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28 and 38-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. § 119**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

**Attachment(s)**

15) ☐ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

## DETAILED ACTION

1. Claims 1-28 and 38-49 are presented for examination. Claims 29-37 have been cancelled by the amendment filed March 26, 2001.

### *Specification*

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### *Claim Rejections*

3. The rejection of claims 1-28 and 38-49 as being anticipated by Atkinson is ***withdrawn***. A new rejection on the merits is now given.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1—5, 16-19 and 38-39 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by a **Direct Rambus Technology Disclosure**.

The **Direct Rambus Technology Disclosure** teaches the invention (claims 1-3, 16-17 and 38) as claimed including a timing circuit in a memory controller within a computer system, with the controller comprising:

a. a memory which is taught as RDRAMs (e.g., see Figure 2);

b. a memory controller which includes a refresh timing circuit for generating clock pulses used to trigger memory refreshes (e.g., see Figure 2 and the section titled 'Features of the Rambus Memory Controller' on page 14);

c. the internal clock generator is taught as part of the chip level device (e.g., see the section titled 'The Physical Layer' on page 8); and,

d. the counters, storage registers and the comparators used for the refresh timing circuit are all common elements which are necessary for such a device to perform its basic functions and are considered inherent to the controller.

As to claim 2, the reference teaches the refresh timing circuit for triggering refresh timing events (e.g., see Figure 4 and the section titled 'Signals' on page 8).

As to claims 4, 19 and 40, the reference inherently teaches a counter for counting the number of clock pulses generated by the clock generator since counters are necessary elements of a controller which performs functions based on clock signals. Refreshes must be performed by specific intervals for any type of DRAM or else the contents are no longer viable.

As to claims 5, 18 and 39, the reference teaches four modes of operation, Nap, Standby, PwrDown and Active. For all of these modes of operation refreshes must be done by a set time frame for the data to be reliable for any type of DRAM.

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 6-15, 20-28 and 40-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over a **Direct Rambus Technology Disclosure**.

The independent claims and intervening claims are taught as given above in the rejection under 35 USC 102(b).

As to claims 6, 20 and 41, the reference does not specifically teach the storage register transmitting the data to the comparator upon a transition from a normal mode to a low power mode. However, the reference does teach a normal mode and a low power mode. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the circuitry include storage registers and comparators for use in going from a normal mode to a low power mode as these are common and necessary elements for use with this type of functionality and circuitry.

As to claims 7, 21-23 and 42-44, the reference inherently teaches a first counter transmitting signals to the comparator whenever the computer system is operating in a low power mode with the signal representing the number of clock pulses received from the clock generator. Even in the low power mode the DRAM must be refreshed by a set number of clock pulses or else the data loses its integrity and is no longer usable.

As to claim 8, the reference inherently teaches transmitting a refresh trigger signal based on the circuitry reaching a specific number of clock pulses.

As to claims 9, 24 and 45, the reference does not specifically teach the refresh timing circuit comprising a second counter, however, counters are notoriously well known in the art and official notice is taken thereof. The claims are not stating a specific connectivity of the various

components or elements, only that these components or elements are being used in the circuitry, however, these uses are the well known common applications of these components or elements.

As to claims 10-11, 25-26 and 46-47, the reference teaches both a normal mode and a low power mode of operation. In order for the system to maintain the refresh functions necessary, the clock pulses must be counted for each mode of operation. Without maintaining a count of the clock pulses, the DRAM cannot be refreshed before the integrity of the data is lost or unnecessary refreshes would occur which would impact the efficiency of the system.

As to claims 12-14, 27-28 and 48-49, the reference does not specifically teach a second counter being deactivated and a first counter being activated whenever the computer system transitions from a normal mode to a low power mode, however, performing refreshes to the RDRAM is taught in all the four modes of operation of the system which means counters must be used to keep track of the clock pulses for all four modes in order to perform the refreshes within the proper intervals. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use counters for counting the clock pulses in the timing circuitry for refreshes because the refreshes are performed during all four modes of operation and counters are common and necessary elements for refresh circuitry and official notice is taken thereof.

As to claim 15, the reference discloses the claimed invention except for the memory being comprised of Extended Data Out Dynamic Random Access Memory (EDO DRAM) and the memory controller therefore being a EDO DRAM controller. It would have been obvious to one of ordinary skill in the art at the time the invention as made to use EDO DRAM because it has been held to be within the general skill of a worker in the art to select a known material on

basis of its suitability for the intended use as a matter of obvious design choice (*In re Leshin*, 125 USPQ 416).

***Response to Applicant's Remarks***

8. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba I. Elmore, whose telephone number is (703) 305-9706. The examiner can normally be reached on M-TH from 7:30 a.m. to 6:00 p.m. EST.

If attempts to reach the examiner by phone fail, the art unit supervisor for 2187, Do Yoo, can be reached for general questions concerning this application at (703) 308-4908. Additionally, the fax phone for Art Unit 2187 is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist at (703) 305-3800/4700.

Reba I. Elmore
Primary Patent Examiner
Art Unit 2187